REMARKS

The office action and references cited therein have been carefully considered together with the present application, and minor amendments have been made to the claims to overcome the claim objections that were made in the office action.

More particularly, claim 2 has been amended to correct the claim in the manner suggested by the examiner. Claim 3 has been amended to recite that the second and third legs are generally perpendicular to the first and second paths, and claim 5 has been amended to change the phrase "may be" to "can be". With regard to the objection to claims 8, 9 and 11, it is believed that the terms "severing", "severed" and "severable" in these claims are not indefinite and that there is not a more appropriate or correct term that can be substituted for the objected to terms. The existing usage is also believed to be explained by the context in which it is used, because the acts of severing or being severed causes a current path to be disconnected from another current path.

The examiner has rejected claims 1-9 and 11-13 under 35 U.S.C. 102(b) as being anticipated by Alpperspach. Applicants respectfully traverse this rejection.

By way of background, the specification at page 1 states that the present invention relates to a design for an access cell and a method for enabling automatic insertion of access cells into an integrated circuit design. As is known to those skilled in the art, an access cell does not perform any of the logical

operations such as AND, OR, NOR, etc., that are carried out by logic cells in the integrated circuit design. A process of designing an integrated circuit may involve insertion of a set of access cells to enable reconfiguration of the integrated circuit in the event that post-fabrication testing reveals a design flaw in the circuit. A detailed discussion of access cells is set forth as background in at pages 1-5.

Alpperspach is directed to a standardized cell layout for large scale integrated circuits that comprises a "masterslice chip" which utilizes ten mask levels, many of which are made in generalized form and which can be thereafter configured during the completion of the manufacturing process to carry out a more specific functionality. Alpperspach utilizes laser cutting and welding tools to make the required inteconnections between certain first and second level conductors as well as to selectively cut first and second level metal conductors at appropriate points to form a complete interconnected grid for a plurality of logic functions. This purports to shorten the lead time for manufacturing LSI chips. It is not directed at all to access cells of the type which are described in the pages 1-4 of the patent application.

As is stated in the specification, access cells are automatically inserted into the integrated circuit design. What is claimed is a current pathway configuration that is quite specifically defined as shown in FIG. 1. This configuration enables the access cells to be inserted in a manner so that that they are usable for their intended purpose, i.e., so that complete route-through is achieved and inserted in a manner that does not adversely affect testing of the

integrated circuit. Additionally, the access cell satisfies minimum spacing requirements associated with the access cell without adversely impacting the overall dimensions of the access cell.

While Alpperspach uses lasers and the like to reconfigure conductors of the integrated circuit, it fails to teach or suggest the specific pathway configuration or the specific location of the cut point and connect points as is set forth in this claim.

More particularly, claim 1 is not anticipated, taught nor suggested by Alpperspach. The examiner has attempted to read Alpperspach on the elements of the claim, stating that the first current path is met by the conductive strip that includes contact points 101 and 102 and that the second current path is met by the adjacent conductive strip that has contact points 103, 104, 113 and 117. Incredibly, the examiner then states that the third current path is the exact identical conductive strip that is identified as the second current path. Clearly, two conductive strips cannot anticipate, teach or suggest three separate current paths which is specifically claimed in claim 1. Additionally, claim 1 states that the third current path has a set of three legs which are then specifically defined and this structure is not even remotely shown, taught or suggested by Alpperspach.

The examiner has also rejected claim 27 as being anticipated by Baxter. Applicants respectfully traverse this rejection. Baxter is directed to a method and apparatus for managing clock timing in an integrated circuit. The whole discussion deals with introducing delay in different clock paths in large

scale integrated circuits. The examiner has identified Fig. 5A and column 5, line 60 through column 6, line 23 which describes the flow chart of the process for inserting and adjusting delay elements to balance clock branches. This is far different from the computer system of claim 27. There is no discussion whatsoever in Baxter about access cells, or that the processor is adapted to modify a netlist to cause a set of nets listed in said netlist to be represented as two unique nets. Because Baxter has nothing to do about access cells, it cannot even remotely teach or suggest modifying a netlist to include a set of access cells, particularly wherein the access cells are defined as being coupled between different ones of two unique nets. Reconsideration and allowance of claim 27 is therefore respectfully requested.

The dependent claims that are dependent upon the independent claims of this application necessarily include the features of the independent claims and intervening claims from which they depend, in addition to reciting other features and/or functionality that is not found in those claims. It is therefore believed that all of the dependent claims are also allowable and reconsideration and allowance of them is respectfully requested.

While the examiner has not objected to the drawings, in the prior prosecution, it was noted that in Fig. 4 reference characters 70 and 72 were both indicated to designate the computer and in Fig. 1 the reference number 27 was missing. Applicants have enclosed an annotated corrected copy of Figs. 1 and 4,

as well as a clean copy of these figures and request that these drawings be accepted.

For the foregoing reasons, reconsideration and allowance of all pending claims is respectfully requested.

Respectfully submitted,

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ADDED 27

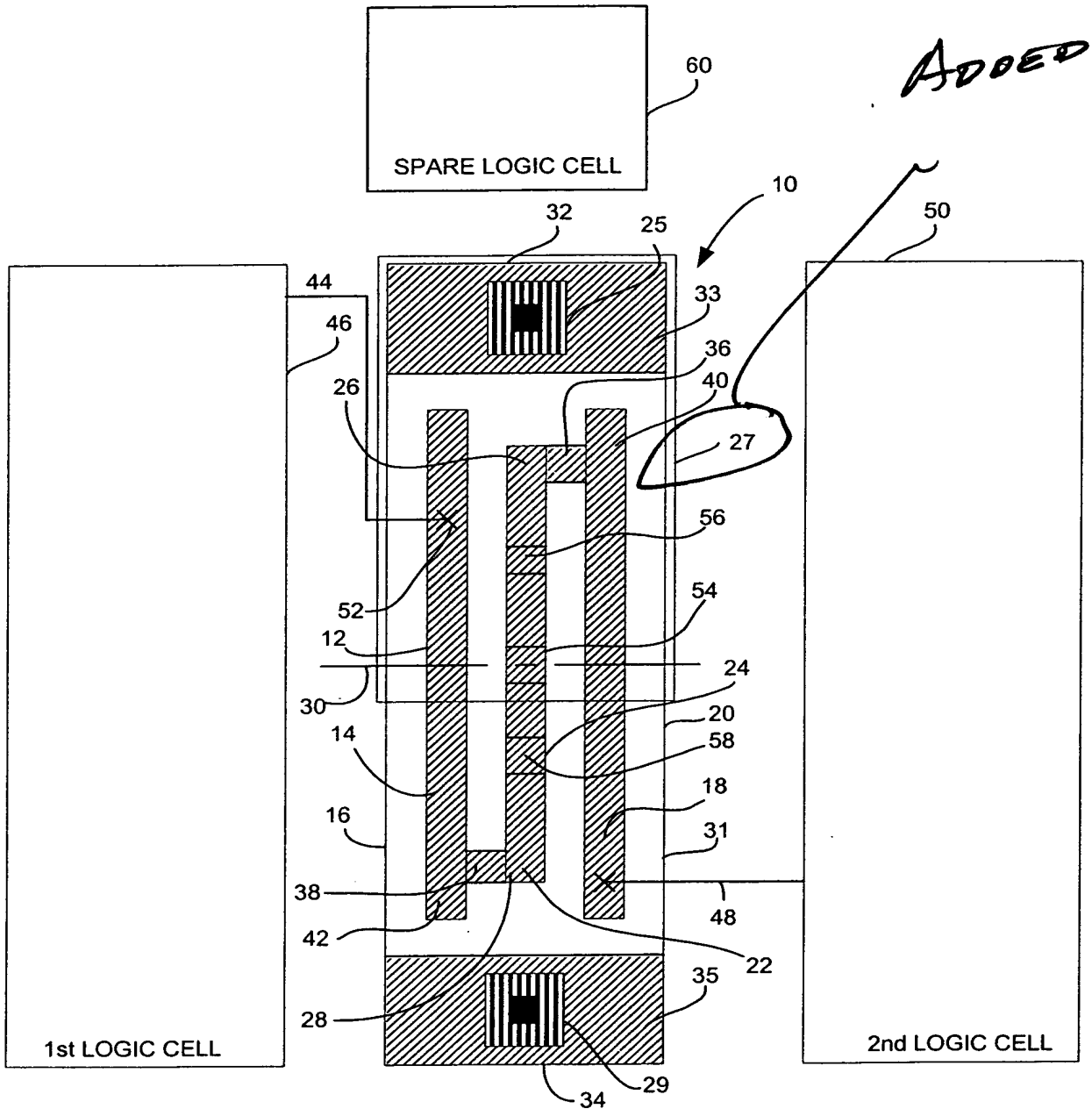

FIG. 1

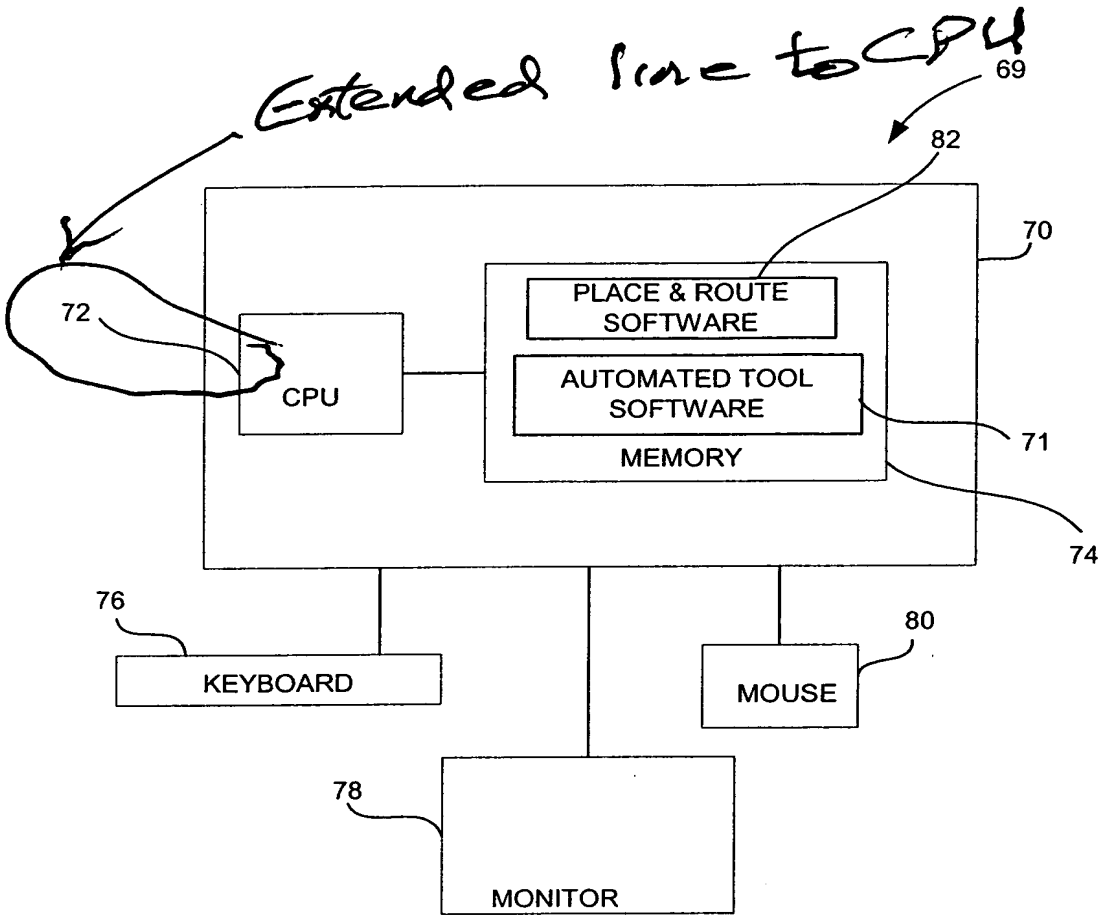
Extended line to CPU
69
82
70
72
PLACE & ROUTE SOFTWARE
AUTOMATED TOOL SOFTWARE
CPU
MEMORY
71
74
76
KEYBOARD
80
MOUSE
78
MONITOR

FIG. 4